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(54) **DATA STORAGE DEVICE COMPENSATING FOR HYSTERETIC RESPONSE OF MICROACTUATOR**

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CPC ***G11B 20/10305*** (2013.01); ***G11B 5/09*** (2013.01); *G11B 5/5552* (2013.01); *G11B 5/59677* (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

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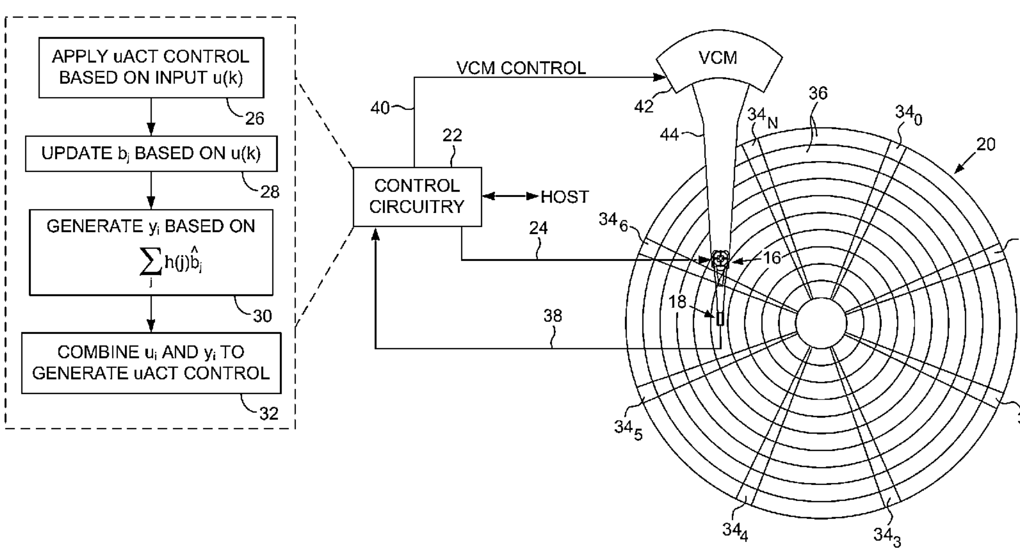
(57) **ABSTRACT**

A data storage device is disclosed comprising a microactuator configured to actuate a head over a disk. A control signal applied to the microactuator is generated based on an input sequence u(k). A Preisach bit map b_j is updated based on the input sequence u(k), wherein the Preisach bit map b_j corresponds to a Preisach plane modeling a hysteretic response of the microactuator. A current compensation value y_i is generated based on an update value generated based on:

$$\sum_j h(j)\hat{b}_j$$

where h_j represents a slice of the Preisach plane and $\hat{b}_j$ is an update bit map based on at least part of the Preisach bit map b_j. The current input u_i and the current compensation value y_i are combined to generate the control signal applied to the microactuator.

26 Claims, 8 Drawing Sheets



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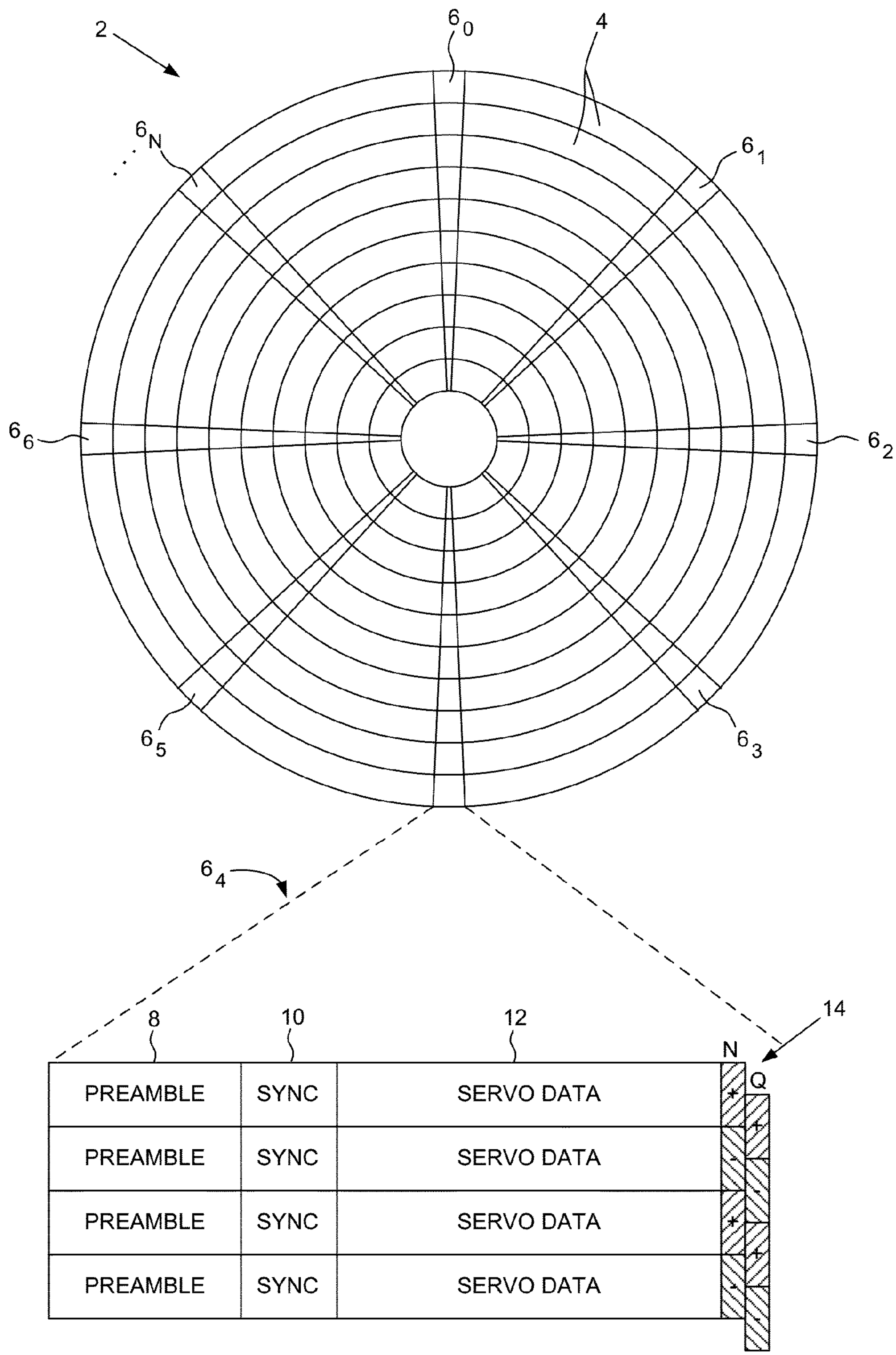


FIG. 1
(Prior Art)

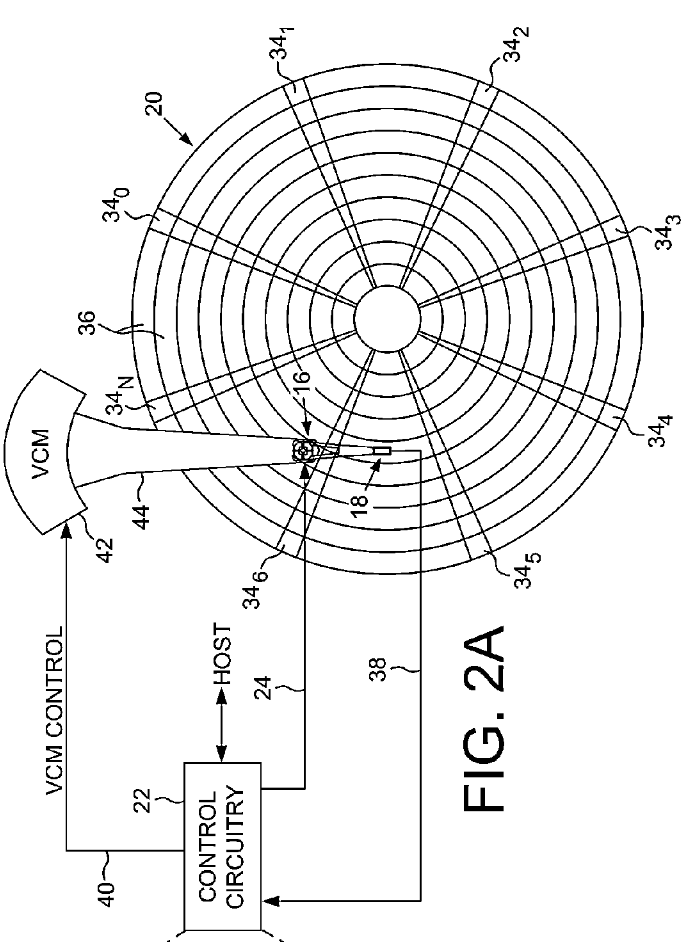


FIG. 2A

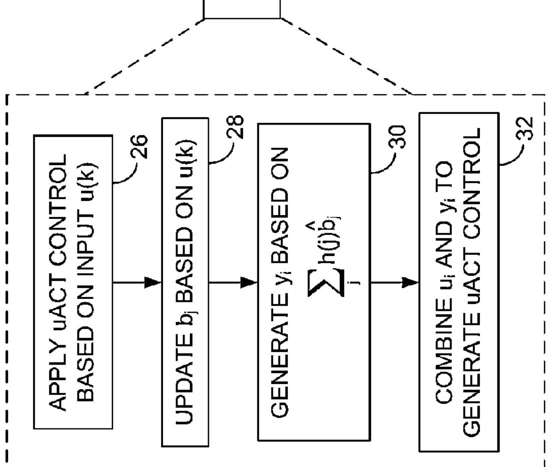


FIG. 2B

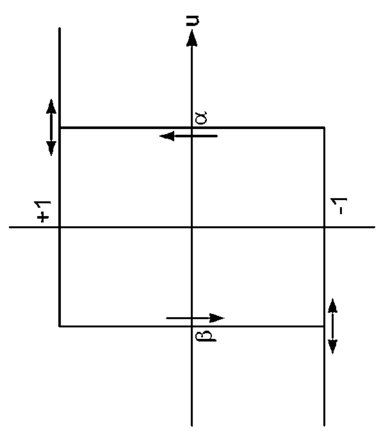


FIG. 2C

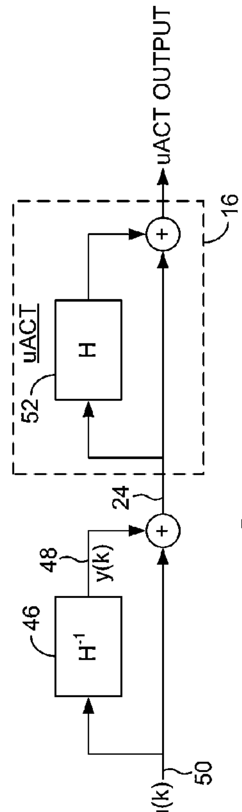


FIG. 2D

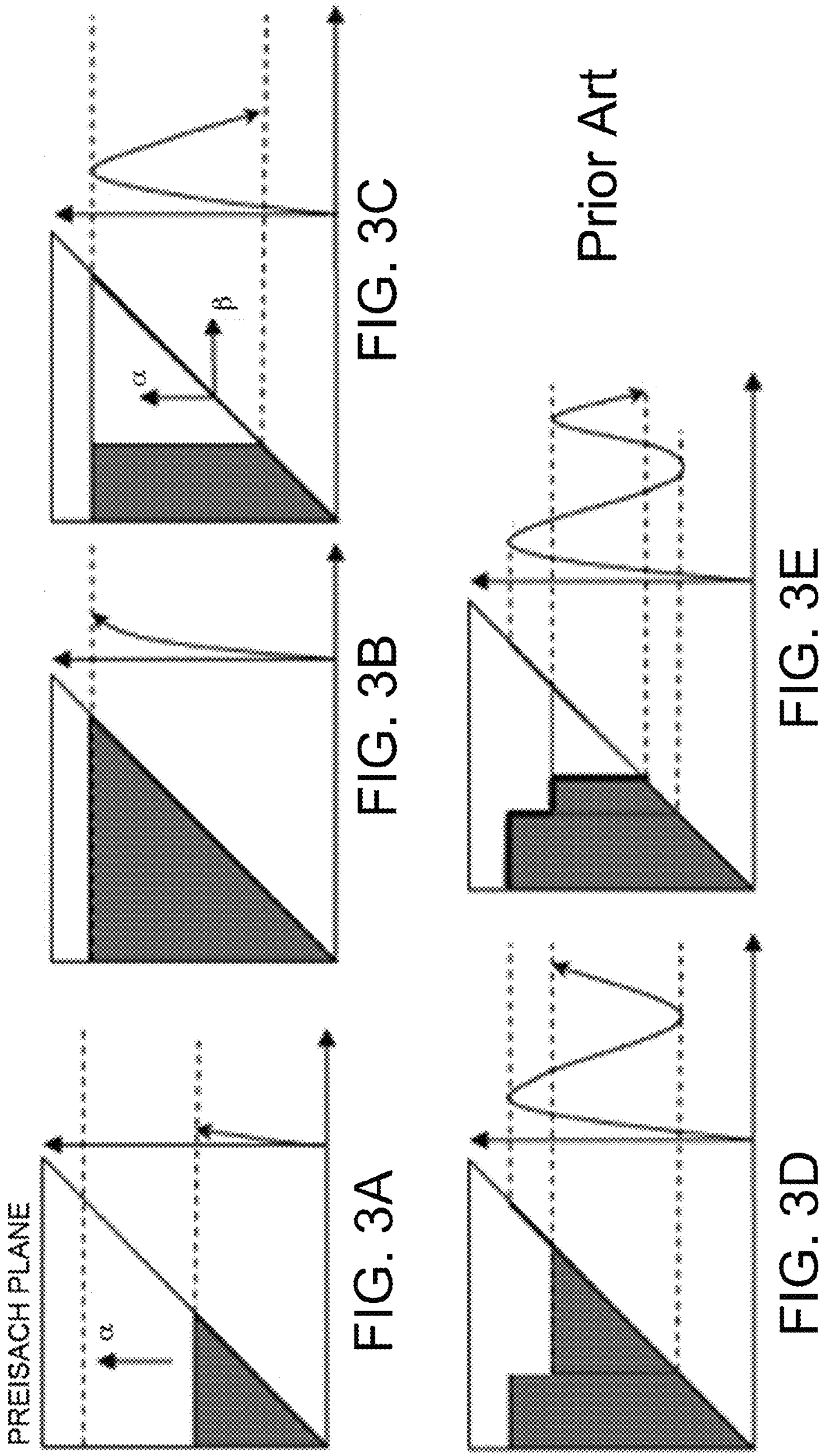


FIG. 3A

FIG. 3B

FIG. 3C

FIG. 3D

FIG. 3E

Prior Art

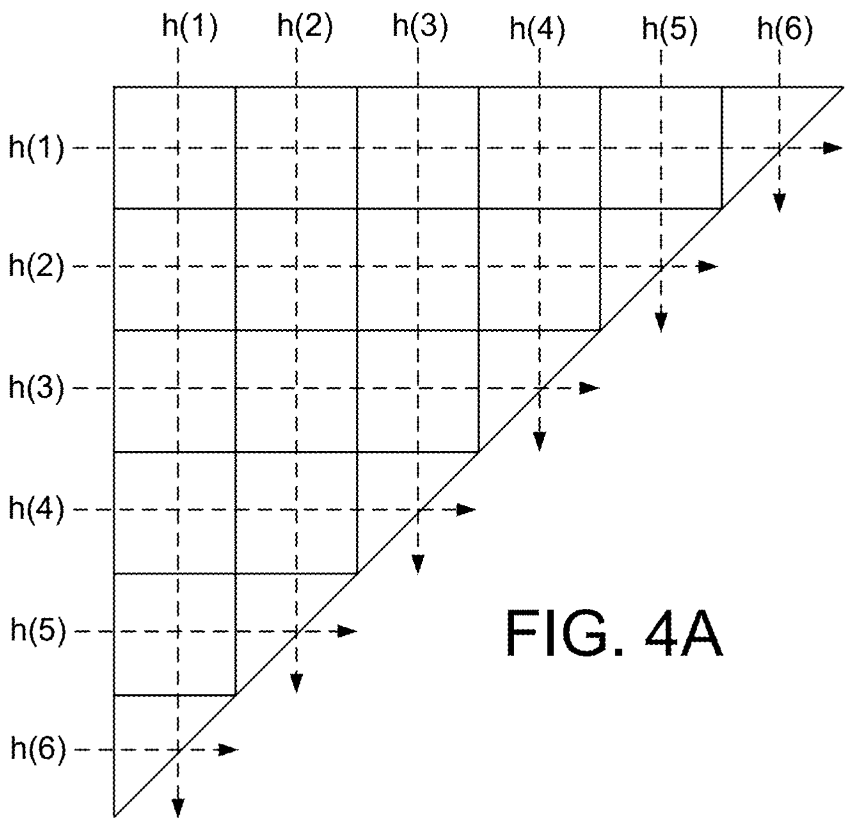


FIG. 4A

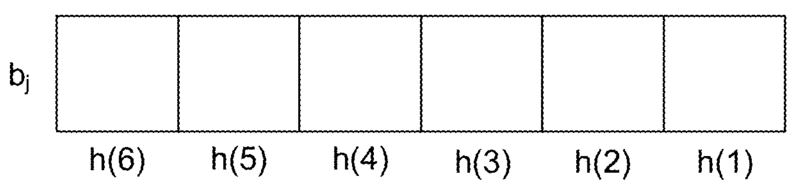


FIG. 4B

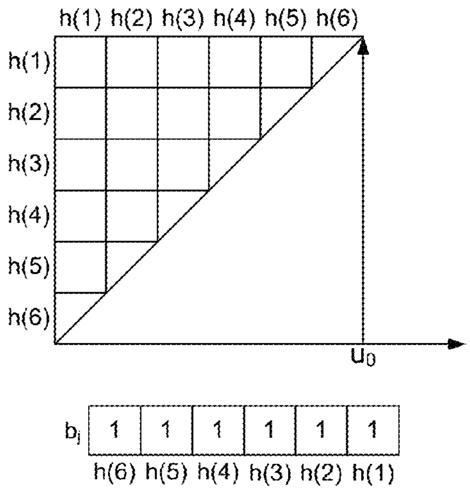


FIG. 5A

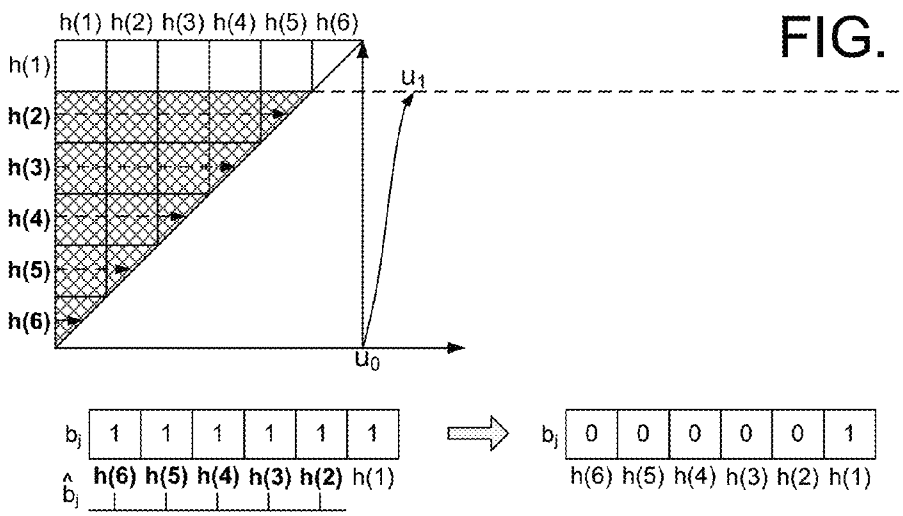


FIG. 5B

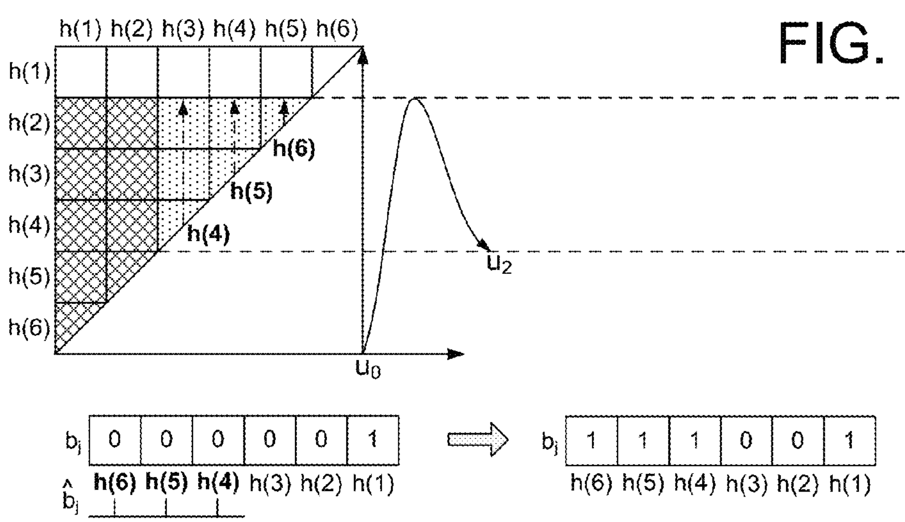


FIG. 5C

FIG. 5D

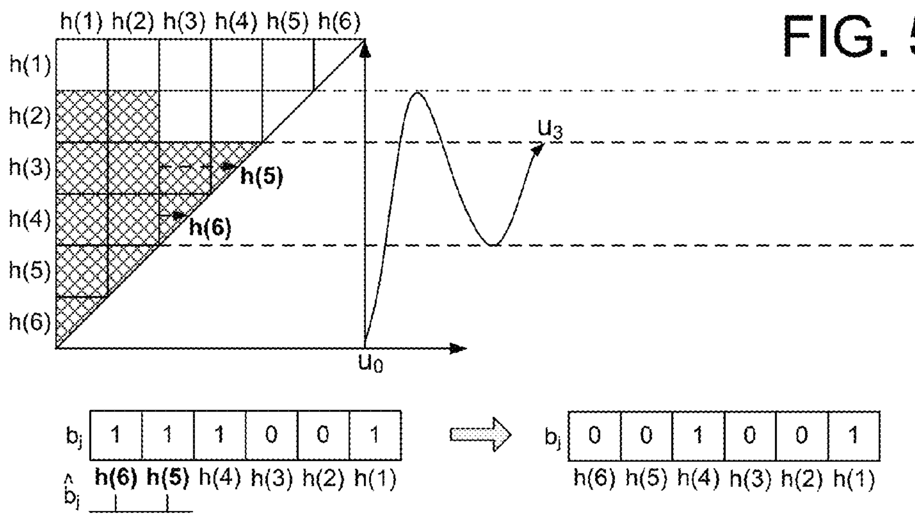


FIG. 5E

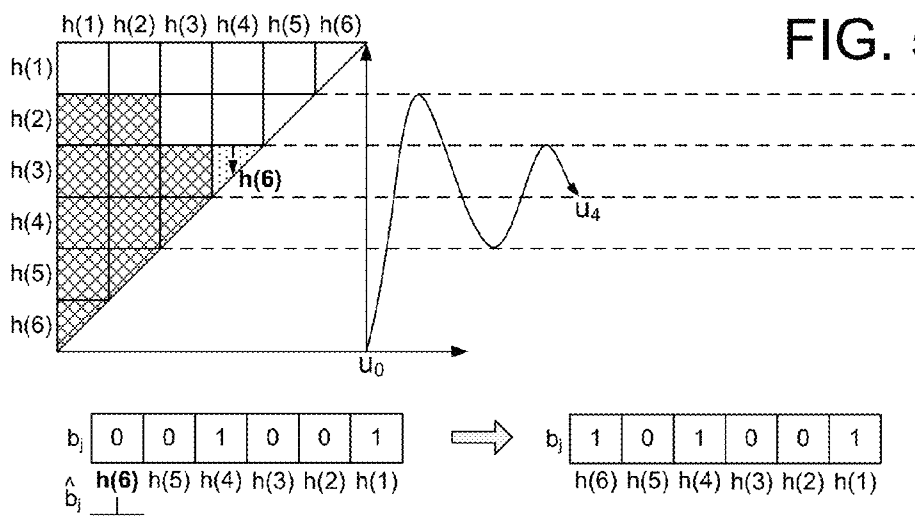
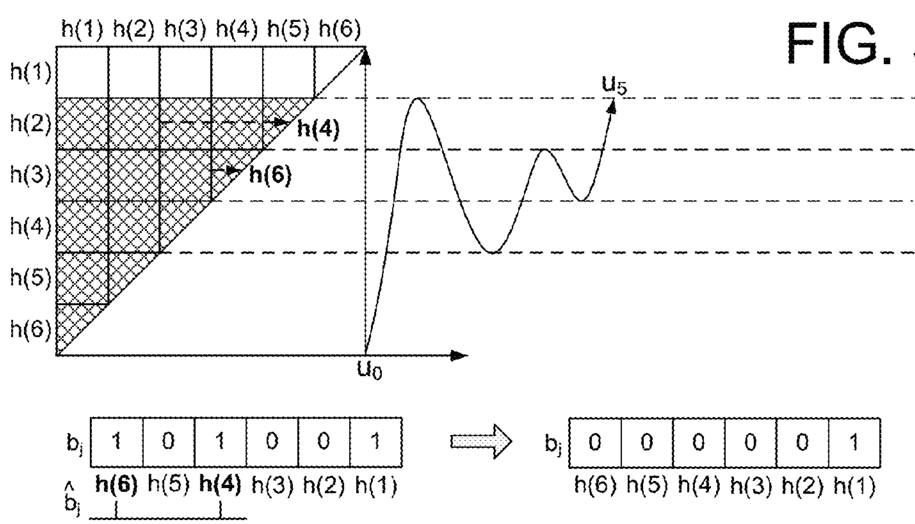


FIG. 5F



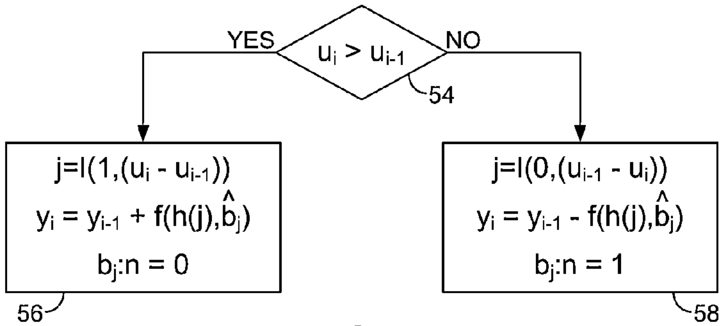


FIG. 6

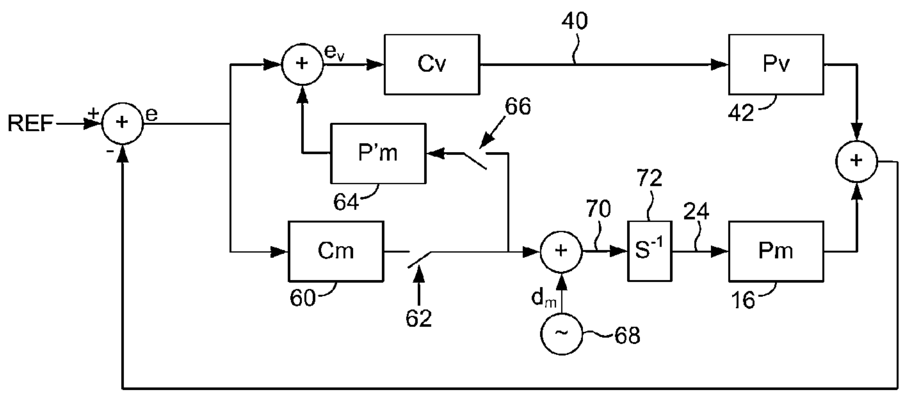


FIG. 7A

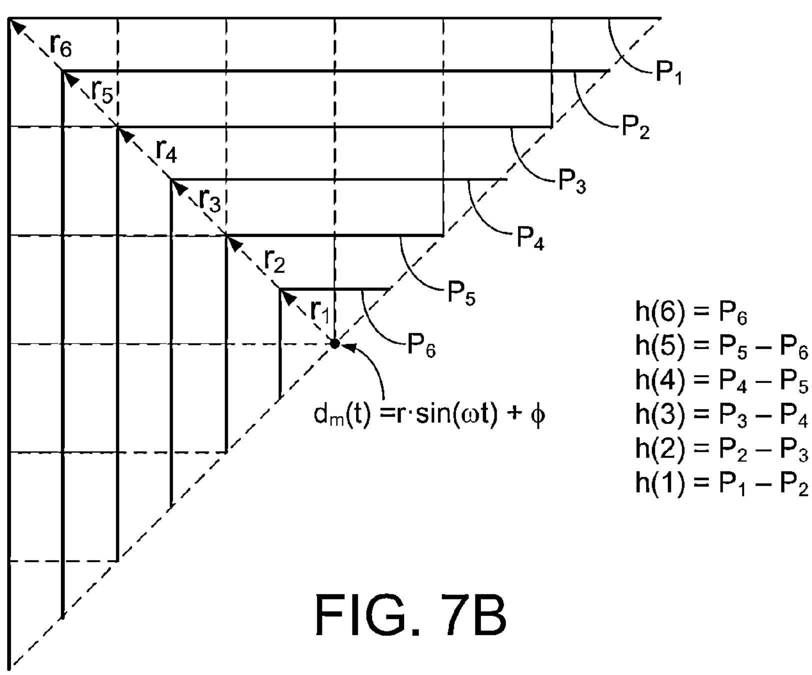
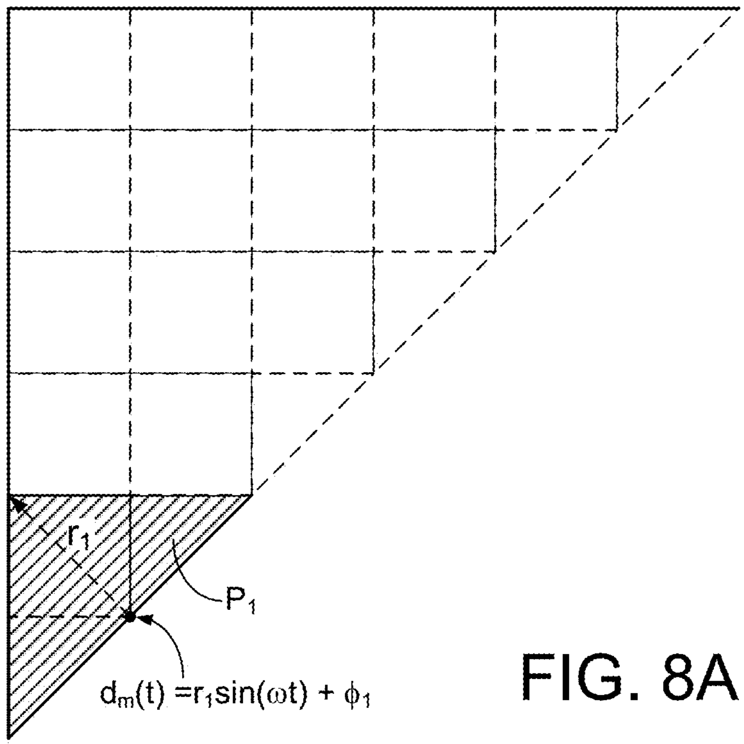
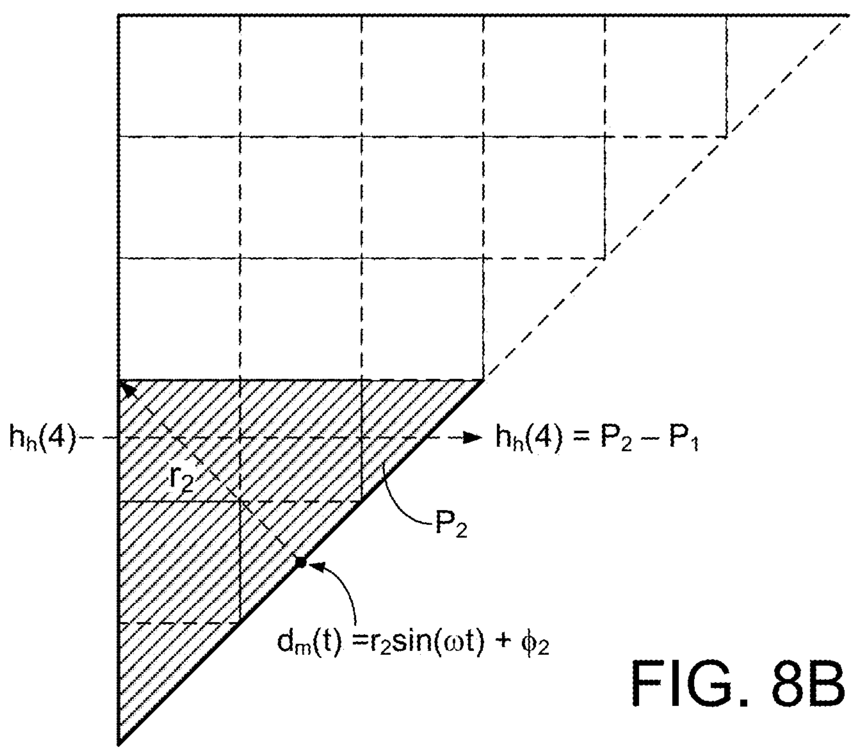


FIG. 7B



r_1
P_1
$d_m(t) = r_1\sin(\omega t) + \phi_1$

FIG. 8A



$h_h(4)$
$h_h(4) = P_2 - P_1$
r_2
P_2
$d_m(t) = r_2\sin(\omega t) + \phi_2$

FIG. 8B

DATA STORAGE DEVICE COMPENSATING FOR HYSTERETIC RESPONSE OF MICROACTUATOR

BACKGROUND

Data storage devices such as disk drives comprise a disk and a head connected to a distal end of an actuator arm which is rotated about a pivot by a voice coil motor (VCM) to position the head radially over the disk. The disk comprises a plurality of radially spaced, concentric tracks for recording user data sectors and servo sectors. The servo sectors comprise head positioning information (e.g., a track address) which is read by the head and processed by a servo control system to control the actuator arm as it seeks from track to track.

FIG. **1** shows a prior art disk format **2** as comprising a number of servo tracks **4** defined by servo sectors $\mathbf{6}_0$-$\mathbf{6}_N$ recorded around the circumference of each servo track. Each servo sector $\mathbf{6}_i$ comprises a preamble **8** for storing a periodic pattern, which allows proper gain adjustment and timing synchronization of the read signal, and a sync mark **10** for storing a special pattern used to symbol synchronize to a servo data field **12**. The servo data field **12** stores coarse head positioning information, such as a servo track address, used to position the head over a target data track during a seek operation. Each servo sector $\mathbf{6}_i$ further comprises groups of servo bursts **14** (e.g., N and Q servo bursts), which are recorded with a predetermined phase relative to one another and relative to the servo track centerlines. The phase based servo bursts **14** provide fine head position information used for centerline tracking while accessing a data track during write/read operations. A position error signal (PES) is generated by reading the servo data **12** and servo bursts **14**, wherein the PES represents a measured position of the head relative to a centerline of a target servo track. A servo controller processes the PES to generate a control signal applied to a head actuator (e.g., a voice coil motor) in order to actuate the head radially over the disk in a direction that reduces the PES.

As the density of the data tracks increases, a microactuator may be employed in combination with the VCM to improve the tracking performance of the servo system. Any suitable microactuator may be employed, such as a suitable piezoelectric (PZT) actuator. The microactuator may actuate the head over the disk in any suitable manner, such as by actuating a suspension relative to a distal end of an actuator arm, or by actuating a slider relative to the suspension.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a prior art disk format comprising servo tracks defined by servo sectors.

FIG. **2**A shows a data storage device in the form of a disk drive according to an embodiment comprising a microactuator configured to actuate a head over a disk.

FIG. **2**B is a flow diagram according to an embodiment wherein a compensation value is generated based on a Preisach bit map.

FIG. **2**C shows a hysteretic response of the microactuator.

FIG. **2**D shows control circuitry according to an embodiment wherein the compensation values compensate for the hysteretic response of the microactuator.

FIGS. **3**A-**3**E illustrate how the Preisach plane can model the position of a microactuator that exhibits hysteresis.

FIG. **4**A shows an embodiment wherein the Preisach plane is quantized into horizontal and vertical slices.

FIG. **4**B shows an example embodiment of a Preisach bit map.

FIGS. **5**A-**5**F illustrate how the compensation values are generated based on the Preisach plane and Preisach bit map according to an embodiment.

FIG. **6** is a flow diagram according to an embodiment for generating the compensation values generated based on the Preisach plane and Preisach bit map according to an embodiment.

FIG. **7**A shows control circuitry according to an embodiment wherein the slices of the Preisach plane are generated by injecting a sinusoid into a control signal applied to the microactuator and measuring a sinusoidal response of the dual stage actuator (DSA) servo loop.

FIG. **7**B illustrates how the slices of the Preisach plane are generated by incrementally increasing the amplitude of the sinusoid injected into the control signal applied to the microactuator.

FIGS. **8**A and **8**B illustrate an embodiment for generating the Preisach plane when the horizontal and vertical slices are asymmetric.

DETAILED DESCRIPTION

FIG. **2**A shows a data storage device in the form of a disk drive according to an embodiment comprising a microactuator **16** configured to actuate a head **18** over a disk **20**. The disk drive further comprises control circuitry **22** configured to execute the flow diagram of FIG. **2**B, wherein a control signal **24** is applied to the microactuator based on an input sequence u(k) (block **26**). A Preisach bit map b_j is updated based on the input sequence u(k) (block **28**), wherein the Preisach bit map b_j corresponds to a Preisach plane modeling a hysteretic response of the microactuator. A current compensation value y_i is generated (block **30**) based on an update value generated based on:

$$\sum_j h(j)\hat{b}_j$$

where h_j represents a slice of the Preisach plane and $\hat{b}_j$ is an update bit map based on at least part of the Preisach bit map b_j. The current input u_i and the current compensation value y_i are combined to generate the control signal applied to the microactuator (block **32**).

In the embodiment of FIG. **2**A, the disk **20** comprises a plurality of servo sectors $\mathbf{34}_0$-$\mathbf{34}_N$ that define a plurality of servo tracks **36**, wherein data tracks are defined relative to the servo tracks at the same or different radial density. The control circuitry **22** processes a read signal **38** emanating from the head **18** to demodulate the servo sectors $\mathbf{34}_0$-$\mathbf{34}_N$ and generate a position error signal (PES) representing an error between the actual position of the head and a target position relative to a target track. The control circuitry **22** filters the PES using a suitable compensation filter to generate a control signal **40** applied to a voice coil motor (VCM) **42** which rotates an actuator arm **44** about a pivot in order to actuate the head **18** radially over the disk **20** in a direction that reduces the PES. The control circuitry **22** also generates the control signal **24** applied to the microactuator **16** in order to actuate the head **18** in fine movements to further reduce the PES. The servo sectors $\mathbf{34}_0$-$\mathbf{34}_N$ may comprise any suitable head position information, such as a track address for coarse positioning and servo bursts for fine positioning. The servo bursts may comprise any suitable pattern, such as an amplitude based servo pattern or a phase based servo pattern.

FIG. **2**C shows an example hysteretic response of the microactuator **16** wherein the position of the microactuator is determined not only by the current control signal **24** but also on a past history of the control signal **24**. FIG. **2**D shows control circuitry according to an embodiment wherein a compensator **46** generates compensation values y(k) **48** that are combined with an input sequence u(k) **50** (based on the PES) to generate the control signal **24** in a manner that compensates for the hysteretic response **52** of the microactuator **16**. In one embodiment, the compensator **46** may generate the compensation values y(k) **48** as the negative of the hysteretic response **52** of the microactuator **16**, and in other embodiments the compensator **46** may implement a more sophisticated algorithm based on the hysteretic response **52** of the microactuator **16**. Accordingly, in one embodiment the hysteretic response **52** of the microactuator **16** is measured, and then the compensator **46** is configured based on the measured hysteretic response.

The hysteretic response **52** of the microactuator **16** may be modeled using a Preisach plane as shown in FIGS. **3**A-**3**E which is represented by the upper triangle with index α and β, respectively. The Preisach model of hysteresis generalizes hysteresis loops as the parallel connection of independent relay hysterons. The input history $\{u_0, u_1, \ldots u_n\}$ projects onto the plane and is recorded as a trajectory T (α, β). The position of the microactuator can be calculated as the integral of the shaded area:

$$y_m(t) = \int\int_{T(\alpha \geq \beta)} \mu(\alpha, \beta) \cdot \hat{\gamma}_{\alpha,\beta}[u(t)]\, d\alpha\, d\beta$$

The position of the microactuator $y_m(t)$ is the integration of its previous trajectory $T(\alpha, \beta)$ on the predefined weighted density plane with weight $\mu(\alpha, \beta)$, multiplied by the hysteron operator $\hat{\gamma}_{\alpha,\beta}[u(t)]$ defined as

$$\hat{\gamma}_{\alpha,\beta}[u(t)] = \begin{Bmatrix} 1, \text{ for increasing } u(t) \\ -1, \text{ for decreasing } u(t) \end{Bmatrix}$$

Referring to the example shown in FIGS. **3**A-**3**E, the shaded area in the triangle increases as the input increases (hysterons turn on), and the shaded area in the triangle decreases as the input decreases (hysterons turn off).

FIG. **4**A shows an embodiment wherein the continuous time Preisach plane described above is quantized into discrete hysterons which are combined to form horizontal and vertical slices $\{h_0, h_1, \ldots h_n\}$ of the Preisach plane. In the example shown in FIG. **4**A, the quantization level is 6 by 6; however, any suitable level of quantization may be employed. In some embodiments, the Preisach plane may be symmetric such that the values representing the horizontal slices are equal to the values representing the vertical slices; however, in other embodiments the Preisach plane may be asymmetric such that the horizontal slices do not equal the vertical slices. FIG. **4**B shows a Preisach bit map b_j that represents the state of the Preisach plane and is described in greater detail with reference to the example shown in FIGS. **5**A-**5**F.

FIG. **5**A shows an initial state of the Preisach plane as well as the Preisach bit map b_j wherein each cell is initialized to a 1-bit which represents an initial position of the microactuator (e.g., center of the stroke with $u_0=0$). FIG. **5**B shows an example of the microactuator position changing due to an increase in the input signal to $u_1=5$ resulting in horizontal slices [h(6),h(5),h(4),h(3),h(2)] of the Preisach plane turning on. Accordingly, the position of the microactuator increases based on:

$$\sum_j h(j)\hat{b}_j$$

where $\hat{b}_j$ is the update bit map based on at least part of the Preisach bit map b_j as illustrated in FIG. **5**B. In this embodiment, since the previous input u_{i-1} is less than the current input u_i, the control circuitry generates the update bit map $\hat{b}_j$ based on the u_i-u_{i-1} high order bits of the Preisach bit map b_j having a target value of 1 (i.e., bits **6**-**2** of the update bit map $\hat{b}_j$ are set to 1 to generate the updated position based on the above equation). The control circuitry then updates the Preisach bit map b_j by inverting these 1-bits to 0-bits as illustrated in FIG. **5**B.

FIG. **5**C shows an example of the microactuator position changing due to a decrease in the input signal to $u_2=2$ resulting in vertical slices [h(6),h(5),h(4)] of the Preisach plane turning off. Accordingly, the position of the microactuator decreases based on:

$$\sum_j h(j)\hat{b}_j$$

where $\hat{b}_j$ is the update bit map based on at least part of the Preisach bit map b_j as illustrated in FIG. **5**C. In this embodiment, since the previous input u_{i-1} is greater than the current input u_i, the control circuitry generates the update bit map $\hat{b}_j$ based on the u_i-u_{i-1} high order bits of the Preisach bit map b_j having a target value of 0 (i.e., bits **6**-**4** of the update bit map $\hat{b}_j$ are set to 1 to generate the updated position based on the above equation). The control circuitry then updates the Preisach bit map b_j by inverting these 0-bits to 1-bits as illustrated in FIG. **5**C.

FIGS. **5**C-**5**F illustrate how the position of the microactuator is updated, as well as how the update bit map $\hat{b}_j$ is generated and the Preisach bit map b_j is updated as the input sequence u(k) changes. In one embodiment, the compensation values y(k) **48** are generated as shown in the flow diagram of FIG. **6** which is understood from the above described process for estimating the hysteretic response **52** of the microactuator. When the previous input u_{i-1} is less than the current input u_i at block **54**, the current compensation value y_i is generated by adding the update value to the previous compensation value y_{i-1} at block **56**. When the previous input u_{i-1} is greater than the current input u_i at block **54**, the current compensation value y_i is generated by subtracting the update value from the previous compensation value y_{i-1} at block **58**. At block **56** the operator j=l(1,k) returns the index in the Preisach bit map of the last kth bit having a value of 1, and at block **58** the operator j=l(0,k) returns the index in the Preisach bit map of the last kth bit having a value of 0.

Any suitable technique may be employed to measure the hysteretic response of the microactuator **16** and to generate the corresponding Preisach plane described above. In one embodiment, a sinusoid is injected into a control signal applied to the microactuator **16**, and a sinusoidal response of the microactuator is measured. In one embodiment, slices of the Preisach plane are generated based on the measured sinusoidal response.

An example of this embodiment is understood with reference to the dual stage actuator (DSA) servo loop shown in FIG. **7**A which comprises a voice coil motor (VCM) servo loop for controlling the VCM **42** and a microactuator servo loop for controlling the microactuator **16**. When measuring the hysteretic response of the microactuator **16**, a microactuator compensator **60** in the microactuator servo loop is disabled by opening switch **62**, and a model of the microactuator **64** is disabled by opening switch **66**. After disabling the microactuator compensator **60**, a sinusoid **68** is injected into control signal **70**, where the sinusoid **68** is of the form:

$$d_m(t)=r\sin(\omega t)+\phi$$

where r represents an amplitude and ϕ represents a DC offset of the sinusoid. The sinusoidal response of the microactuator $y_m(t)$ may be represented as:

$$y_m(t)=K[d_m(t)+\tilde{H}(d_m(t))]$$

where K represents a gain of the microactuator, $\tilde{H}(d_m(t))=S^{-1}H(d_m(t))$ represents a residue hysteretic response after static non-linear compensation **72** of the microactuator, and $H(d_m(t))$ represents the original hysteretic response of the microactuator based on the past input history. In one embodiment, the hysteretic response of the microactuator may be estimated by computing a discrete Fourier transform (DFT) of the microactuator response Y_m after injecting the above input sinusoid as:

$$\left|\tilde{H}(j\omega)\right| = \frac{Y_m - KD_m}{K}$$

Accordingly by injecting a sinusoid **68** into the control signal **70** and measuring the sinusoidal response of the microactuator, the hysteretic response of the microactuator may be estimated based on the above equation. In one embodiment, by varying the amplitude r (and optionally the offset ϕ) of the input sinusoid **68** the entire Preisach plane described above may be characterized.

In one embodiment, the Preisach plane may be symmetric meaning that the horizontal slices shown in FIG. **4**A are equal in value to the vertical slices (and the hysterons of the Preisach plane have the same value). In this embodiment, the Preisach plane may be characterized by measuring the hysteretic response of the microactuator at varying amplitudes r of the input sinusoid **68**, and at a fixed offset ϕ corresponding to the middle coordinate along the diagonal as shown in FIG. **7**B. At a first amplitude r_1 of the input sinusoid a first triangle area P_6 of the Preisach plane may be generated as described above, where this area P_6 corresponds to the h(6) slice (horizontal and vertical) of the Preisach plane. At the second amplitude r_2 of the input sinusoid a second triangle area P_5 of the Preisach plane may be measured as described above, where the h(5) slice corresponds to P_5-P_6. This process is repeated until all six slices of the Preisach plane have been generated as illustrated in FIG. **7**B.

In one embodiment, the hysteretic response of the microactuator **16** may correspond to an asymmetric Preisach plane such that the horizontal and vertical slices shown in FIG. **4**A may have different values. In order to characterize an asymmetric Preisach plane, in one embodiment both the amplitude r and the offset ϕ of the input sinusoid **68** shown in FIG. **7**A are varied. An example of this embodiment is illustrated in FIGS. **8**A and **8**B, wherein in FIG. **8**A the input sinusoid **68** has a first amplitude r_1 and a first offset ϕ_1 in order to measure the triangle area P_1 of the Preisach plane. In FIG. **8**B the input sinusoid **68** has a second amplitude r_2 and as second offset ϕ_2 in order to measure the triangle area P_2 of the Preisach plane. The horizontal slice $h_h(4)$ of the Preisach plane may then be generated as P_2-P_1. A similar process may be used to measure each of the horizontal and vertical slices of the Preisach plane, and in one embodiment a similar process may be used to measure each hysteron in the Preisach plane in the event that each hysteron has a different value.

Any suitable microactuator may be employed to actuate the head over the disk, such as a piezoelectric actuator. In addition, the microactuator may actuate the head over the disk in any suitable manner, such as by actuating a suspension relative to the actuator arm, or by actuating a head gimbal assembly (HGA) that couples a slider to the suspension.

Any suitable control circuitry may be employed to implement the flow diagrams in the above embodiments, such as any suitable integrated circuit or circuits. For example, the control circuitry may be implemented within a read channel integrated circuit, or in a component separate from the read channel, such as a disk controller, or certain operations described above may be performed by a read channel and others by a disk controller. In one embodiment, the read channel and disk controller are implemented as separate integrated circuits, and in an alternative embodiment they are fabricated into a single integrated circuit or system on a chip (SOC). In addition, the control circuitry may include a suitable preamp circuit implemented as a separate integrated circuit, integrated into the read channel or disk controller circuit, or integrated into a SOC.

In one embodiment, the control circuitry comprises a microprocessor executing instructions, the instructions being operable to cause the microprocessor to perform the flow diagrams described herein. The instructions may be stored in any computer-readable medium. In one embodiment, they may be stored on a non-volatile semiconductor memory external to the microprocessor, or integrated with the microprocessor in a SOC. In another embodiment, the instructions are stored on the disk and read into a volatile semiconductor memory when the disk drive is powered on. In yet another embodiment, the control circuitry comprises suitable logic circuitry, such as state machine circuitry.

In various embodiments, a disk drive may include a magnetic disk drive, an optical disk drive, etc. In addition, while the above examples concern a disk drive, the various embodiments are not limited to a disk drive and can be applied to other data storage devices and systems, such as magnetic tape drives, solid state drives, hybrid drives, etc. In addition, some embodiments may include electronic devices such as computing devices, data server devices, media content storage devices, etc. that comprise the storage media and/or control circuitry as described above.

The various features and processes described above may be used independently of one another, or may be combined in various ways. All possible combinations and subcombinations are intended to fall within the scope of this disclosure. In addition, certain method, event or process blocks may be omitted in some implementations. The methods and processes described herein are also not limited to any particular sequence, and the blocks or states relating thereto can be performed in other sequences that are appropriate. For example, described tasks or events may be performed in an order other than that specifically disclosed, or multiple may be combined in a single block or state. The example tasks or events may be performed in serial, in parallel, or in some other manner. Tasks or events may be added to or removed from the disclosed example embodiments. The example systems and components described herein may be configured differently than described. For example, elements may be added to, removed from, or rearranged compared to the disclosed example embodiments.

While certain example embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions disclosed herein. Thus, nothing in the foregoing description is intended to imply that any particular feature, characteristic, step, module, or block is necessary or indispensable. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the embodiments disclosed herein.

What is claimed is:

1. A data storage device comprising:

a disk;

a head;

a microactuator configured to actuate the head over the disk; and

control circuitry configured to:

generate a control signal applied to the microactuator based on an input sequence u(k);

update a Preisach bit map b_j based on the input sequence u(k), wherein the Preisach bit map b_j corresponds to a Preisach plane modeling a hysteretic response of the microactuator;

generate a current compensation value y_i based on an update value generated based on:

$$\sum_j h(j)\hat{b}_j$$

where h_j represents a slice of the Preisach plane and $\hat{b}_j$ is an update bit map based on at least part of the Preisach bit map b_j; and

combine a current input u_i and the current compensation value y_i to generate the control signal applied to the microactuator.

2. The data storage device as recited in claim **1**, wherein the compensation value compensates for the hysteretic response of the microactuator.

3. The data storage device as recited in claim **1**, wherein when a previous input u_{i-1} is less than the current input u_i, the control circuitry is further configured to generate the current compensation value y_i by adding the update value to a previous compensation value y_{i-1}.

4. The data storage device as recited in claim **1**, wherein when a previous input u_{i-1} is less than the current input u_i, the control circuitry is further configured to generate the update bit map $\hat{b}_j$ based on u_i-u_{i-1} bits of the Preisach bit map b_j.

5. The data storage device as recited in claim **4**, wherein the u_i-u_{i-1} bits of the Preisach bit map b_j comprise high order bits of the Preisach bit map b_j having a target value.

6. The data storage device as recited in claim **5**, wherein the u_i-u_{i-1} bits of the Preisach bit map b_j comprise the high order bits of the Preisach bit map b_j having a target value of 1.

7. The data storage device as recited in claim **6**, wherein after generating the update value the control circuitry is further configured to clear m high order bits of the Preisach bit map b_j where m represents the u_i-u_{i-1} high order bits of the Preisach bit map b_j having a target value of 1 plus the intervening 0 bits.

8. The data storage device as recited in claim **1**, wherein when a previous input u_{i-1} is greater than the current input u_i, the control circuitry is further configured to generate the current compensation value y_i by subtracting the update value from a previous compensation value y_{i-1}.

9. The data storage device as recited in claim **1**, wherein when a previous input u_{i-1} is greater than the current input u_i, the control circuitry is further configured to generate the update bit map $\hat{b}_j$ by inverting at least part of the Preisach bit map b_j.

10. A data storage device comprising:

a head;

a disk;

a microactuator configured to actuate the head over the disk; and

control circuitry configured to:

inject a sinusoid into a control signal applied to the microactuator and measure a sinusoidal response of the microactuator; and

generate a Preisach plane based on at least two cycles of the measured sinusoidal response, wherein the Preisach plane models a hysteretic response of the microactuator.

11. The data storage device as recited in claim **10**, wherein the control circuitry is further configured to:

generate a control signal applied to the microactuator based on an input sequence u(k);

generate compensation values y(k) based on the input sequence u(k) and the Preisach plane; and

combine a current input u_i and a current compensation value y_i to generate the control signal applied to the microactuator.

12. The data storage device as recited in claim **11**, wherein the compensation values y(k) compensate for the hysteretic response of the microactuator.

13. The data storage device as recited in claim **10**, wherein the control circuitry is further configured to:

adjust an offset of the sinusoid injected into the control signal applied to the microactuator; and

after adjusting the offset, generate part of the Preisach plane based on at least two cycles of the measured sinusoidal response.

14. A method of operating a data storage device, the method comprising:

generating a control signal applied to a microactuator based on an input sequence u(k), wherein the microactuator is configured to actuate a head over a disk;

updating a Preisach bit map b_j based on the input sequence u(k), wherein the Preisach bit map b_j corresponds to a Preisach plane modeling a hysteretic response of the microactuator;

generating a current compensation value y_i based on an update value generated based on:

$$\sum_j h(j)\hat{b}_j$$

where h_j represents a slice of the Preisach plane and $\hat{b}_j$ is an update bit map based on at least part of the Preisach bit map b_j; and combining a current input u_i and the current compensation value y_i to generate the control signal applied to the microactuator.

15. The method as recited in claim **14**, wherein the compensation value compensates for the hysteretic response of the microactuator.

16. The method as recited in claim **14**, wherein when a previous input u_{i-1} is less than the current input u_i, the method further comprises generating the current compensation value y_i by adding the update value to a previous compensation value y_{i-1}.

17. The method as recited in claim **14**, wherein when a previous input u_{i-1} is less than the current input u_i, the method further comprises generating the update bit map $\hat{b}_j$ based on u_i-u_{i-1} bits of the Preisach bit map b_j.

18. The method as recited in claim **17**, wherein the u_i-u_{i-1} bits of the Preisach bit map b_j comprise high order bits of the Preisach bit map b_j having a target value.

19. The method as recited in claim **18**, wherein the u_i-u_{i-1} bits of the Preisach bit map b_1 comprise the high order bits of the Preisach bit map b_1 having a target value of 1.

20. The method as recited in claim **19**, wherein after generating the update value the method further comprises clearing m high order bits of the Preisach bit map b_j where m represents the u_i-u_{i-1} high order bits of the Preisach bit map b_j having a target value of 1 plus the intervening 0 bits.

21. The method as recited in claim **14**, wherein when a previous input u_{i-1} is greater than the current input u_i, the method further comprises generating the current compensation value y_i by subtracting the update value from a previous compensation value y_{i-1}.

22. The method as recited in claim **14**, wherein when a previous input u_{i-1} is greater than the current input u_i, the method further comprises generating the update bit map $\hat{b}_j$ by inverting at least part of the Preisach bit map b_j.

23. A method of operating a data storage device, the method comprising:

actuating a head over a disk using a microactuator;

injecting a sinusoid into a control signal applied to the microactuator and measure a sinusoidal response of the microactuator; and

generating a Preisach plane based on at least two cycles the measured sinusoidal response, wherein the Preisach plane models a hysteretic response of the microactuator.

24. The method as recited in claim **23**, further comprising:

generating a control signal applied to the microactuator based on an input sequence u(k);

generating compensation values y(k) based on the input sequence u(k) and the Preisach plane; and

combining a current input u_i and a current compensation value y_i to generate the control signal applied to the microactuator.

25. The method as recited in claim **24**, wherein the compensation values y(k) compensate for the hysteretic response of the microactuator.

26. The method as recited in claim **23**, further comprising:

adjusting an offset of the sinusoid injected into the control signal applied to the microactuator; and

after adjusting the offset, generating part of the Preisach plane based on at least two cycles the measured sinusoidal response.

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